Power Quality Improvement Using a Power Electronic Transformer Based DVR

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***Abstract*— In this paper a three-phase four-wire Dynamic Voltage Restorer (DVR) with bi-directional power electronic transformer structure is proposed to inject required compensating series voltage to the electric power system in such a way that continuous sinusoidal voltage is seen at load side ever at heavy fault occurrences at utility side. The proposed structure is composed of a three-phase four-leg inverter, three single-phase high frequency transformers, three cycloconverters and high frequency harmonic filter that are connected to the utility. Three dimensional space vector modulation (3DSVM) method is used for pulse generation. Fourth added wire enables the DVR to compensate unbalance voltage disturbance that are custom power quality problems in electrical utility. The performance of the structure and applied switching scheme are verified under both balanced and unbalanced disturbances via simulation study in PSCAD/EMTDC software.**

Keywords—PET; DVR; 3DSVM; power quality;

I. INTRODUCTION

Power quality problem is one of the major concerns in power distribution system. Consumer's equipment need pure balanced sinusoidal voltage with constant root mean square (RMS) value to have their satisfying operation. Any voltage waveform disturbances may cause serious faults in electrical equipment. Nowadays with advent of advanced electrical and electronic equipment, there has been a progressive need to high quality electric power. One of the equipment that mitigates the power quality problems is dynamic voltage restorer (DVR). DVR is a series compensator which is able to protect a sensitive load from the distortion at the utility side during fault or over load in power system [1-4]. The basic principle of a series compensator is simple. The series compensator can restore the load side voltage to the desired amplitude and waveform, by injecting a controlled series voltage, even when the source voltage is unbalanced or distorted. In many structure of conventional DVR, the transformer is used to increase the input voltage and achieve desired output voltage level. Also this transformer can provide the galvanic isolation, but at power frequencies, isolation transformers have some drawbacks, such as heavy weight, large size and high cost [5]. The use of power electronic transformer (PET) is a solution to overcome the aforementioned disadvantages. PET is a new type of power transformer which has the advantage of increasing of the frequency to reduce the size. Application of high frequency transformers increases the power density and reduces the overall cost of the system. Recently, different topologies in literature have been presented [6-8]. The concept of high-frequency-link DVR for a single-phase system has been proposed [9]. In this paper, PET based distributed DVR for load side protection against voltage disturbance is investigated in PSCAD/EMTDC simulation package. In practical cases, the sags and swells can be unbalanced. Therefore, the DVR should be able to inject unbalanced three-phase voltages. These voltages may be generated by the three-phase four-wire converters with split capacitor [10] or H-bridge inverters [11].

Based on the aforementioned discussions, this paper proposes a PET based three-phase four-wire DVR to inject required compensating series voltage to the power system in such a way that continuous sinusoidal voltage is seen at load side ever at heavy fault occurrences at utility side. The proposed structure is composed of a three-phase four-leg inverter, three single-phase high frequency transformers and a three-phase high frequency harmonic filter that are connected to the utility.

II. CIRCUIT CONFIGURATION

Three dimensional space vector modulation (3DSVM) is applied to the proposed DVR to generate switching pulses for power switches. Fourth added wire enables the DVR to compensate unbalance voltage sag and swell that are custom power quality problems in electrical utility. The aim of this paper is to propose a new approach solution to provide voltage quality for sensitive loads under balanced and unbalanced disturbance. This can be done by a three-phase four-leg converter based on 3DSVM. This technique has some advantages such as higher amplitude modulation indexes if compared with convectional SPWM techniques [12]. The proposed DVR is shown in Fig. 1. The purpose of control scheme is to maintain the load voltage at a desired value. In order to control the three-phase four-wire inverter, 3DSVM method is used that has some advantages such as more efficiency, high DC link voltage utilization, lower output voltage THD, less switching and conduction losses, wide linear modulation range, more output voltage magnitude and its simple digital implementation [12]. The block diagram of the control system used is shown in Fig. 2.

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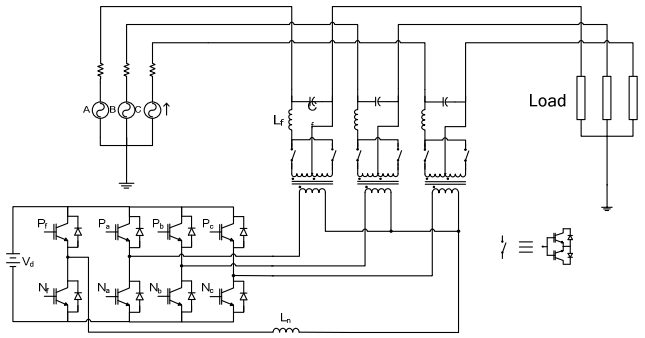


Fig. 1. Three-Phase Four-Wire DVR

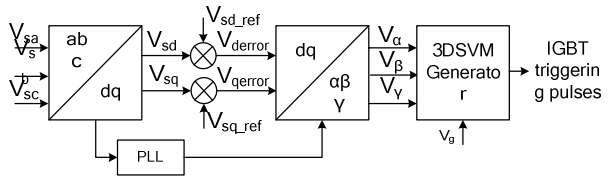


Fig. 2. Control block diagram of DVR

This algorithm is based on the representation of the natural coordinates a, b and c in a new 3-D orthogonal frame, called α–β–γ frame, that is as bellow

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_\gamma \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (1)$$

The switching combinations can be represented by the ordered sets [S_a, S_b, S_c, S_f] that are shown in Fig. 3, where S_a=*p* denotes the upper switch in phase A, S_{ap} is closed, and S_a=*n* denotes the bottom switch in phase A, S_{an} is closed. The same notation applies to phase legs B and C and to the fourth leg. Fig. 4 represents the general case of the four legs inverter switching vectors in α–β–γ frame. There are two zero switching vectors (ZSV) that located at the origin of the α–β–γ coordinate and fourteen non-zero switching vectors (NZSV). Seven vectors are located in the positive part of the γ axis, while seven other vectors are found in the negative part. The line to neutral voltage for all sixteen switching combinations in a–b–c and α–β–γ coordinates is shown in Table I and Table II, respectively.

A. Selection of Switching Vectors

In order to minimize the circulating energy and to reduce the current ripple, switching vectors adjacent to the reference vector should be selected. This is because that the adjacent switching vectors produce non conflicting voltage pulses. The position of the reference space vector can be determined in two steps:

- The first step is prism determination. Totally, there are six prisms that the flowchart in Fig. 5 explains their selection.
- Determination of the tetrahedron in which the reference vector is located. Each prism contains four tetrahedrons that are shown in Fig. 6 (for prism 1). The reference space vector is located based on the polarity of the reference space vector components in a–b–c frame that is given in Table III.

B. Projection of the Reference Vector

The time duration of the selected switching vector can be easily computed by projecting the reference vector in to the adjacent NSZVs.

The corresponding duty ratios of the switching vectors are given by:

$$V_{ref} = d_1 V_1 + d_2 V_2 + d_3 V_3 \quad (2)$$

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} = \frac{1}{V_g}\begin{bmatrix} 1 & 0 & 1 \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} & -1 \\ 0 & \sqrt{3} & 0 \end{bmatrix}\begin{bmatrix} V_{\alpha\_ref} \\ V_{\beta\_ref} \\ V_{\gamma\_ref} \end{bmatrix} \quad (3)$$

$$d_Z = 1 - d_1 - d_2 - d_3 \quad (4)$$

$$\alpha + \beta = \chi. \quad (1) \quad (1)$$

For the reference vector in other tetrahedrons, only the projection matrix should be changed in (3).Complete table for the corresponding NZSVs and matrices to compute the duty ratios of all 24 tetrahedrons is given in [12].

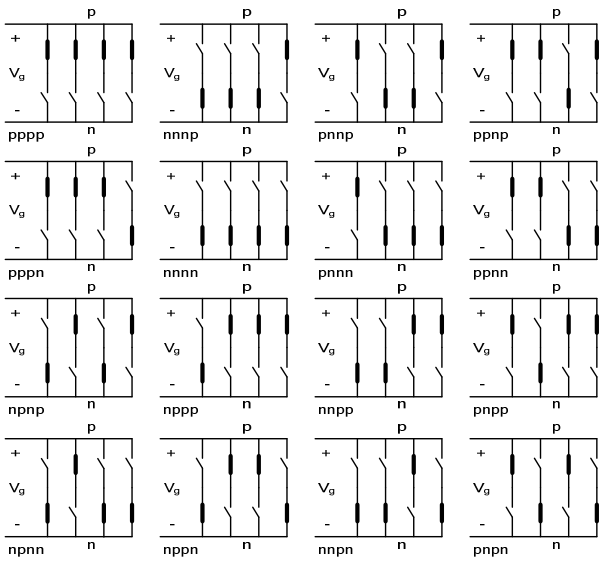


Fig. 3. Possible switching combinations

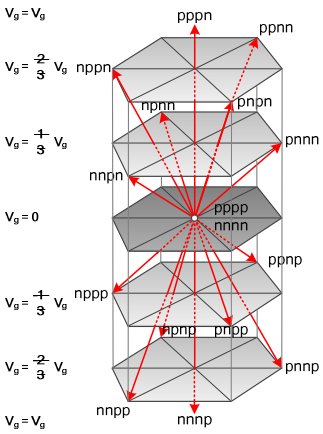


Fig. 4. Switching vectors in α–β–γ coordinate

TABLE I. The four-leg inverter switching network ac terminal voltages

	pppp	*nnnp*	*pnnp*	*ppnp*	*npnp*	*nppp*	*nnpp*	*pnpp*
V_{af}	0	$-V_g$	0	0	$-V_g$	$-V_g$	$-V_g$	0
V_{bf}	0	$-V_g$	$-V_g$	0	0	0	$-V_g$	$-V_g$
V_{cf}	0	$-V_g$	$-V_g$	$-V_g$	$-V_g$	0	0	0
	pppn	*nnnn*	*pnnn*	*ppnn*	*npnn*	*nppn*	*nnpn*	*pnpn*
V_{af}	V_g	0	V_g	V_g	0	0	0	V_g
V_{bf}	V_g	0	0	0	V_g	V_g	0	0
V_{cf}	V_g	0	0	0	0	V_g	V_g	V_g

TABLE II. Inverter voltages in the α–β–γ coordinate

	pppp	*nnnp*	*pnnp*	*ppnp*	*npnp*	*nppp*	*nnpp*	*pnpp*
V_α	0	0	$\frac{2}{3}V_g$	$\frac{1}{3}V_g$	$\frac{-1}{3}V_g$	$\frac{-2}{3}V_g$	$\frac{-1}{3}V_g$	$\frac{1}{3}V_g$
V_β	0	0	0	$\frac{1}{\sqrt{3}}V_g$	$\frac{1}{\sqrt{3}}V_g$	0	$\frac{-1}{\sqrt{3}}V_g$	$\frac{-1}{\sqrt{3}}V_g$
V_γ	0	-V_g	$\frac{-2}{3}V_g$	$\frac{-1}{3}V_g$	$\frac{-2}{3}V_g$	$\frac{-1}{3}V_g$	$\frac{-2}{3}V_g$	$\frac{-1}{3}V_g$
	pppn	nnnn	pnnn	ppnn	npnn	nppn	nnpn	pnpn
V_α	0	0	$\frac{2}{3}V_g$	$\frac{1}{3}V_g$	$\frac{-1}{3}V_g$	$\frac{-2}{3}V_g$	$\frac{-1}{3}V_g$	$\frac{1}{3}V_g$
V_β	0	0	0	$\frac{1}{\sqrt{3}}V_g$	$\frac{1}{\sqrt{3}}V_g$	0	$\frac{-1}{\sqrt{3}}V_g$	$\frac{-1}{\sqrt{3}}V_g$
V_γ	V_g	0	$\frac{1}{3}V_g$	$\frac{2}{3}V_g$	$\frac{1}{3}V_g$	$\frac{2}{3}V_g$	$\frac{1}{3}V_g$	$\frac{2}{3}V_g$

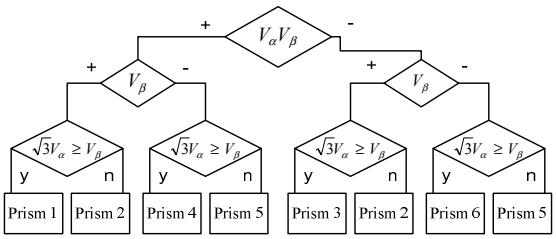


Fig. 5. Flowchart used to determine prism information

C. Sequencing Scheme of Switching Vectors

The selection of ZSVs and the sequencing of switching vectors involve trade-off between losses and harmonic distortion and they can be optimized for different applications.

In order to implement of 3DSVM with high frequency transformer, it should be changed in conventional sequencing scheme. The sequencing scheme of the proposed DVR is shown in Fig.7. It should be noticed that the notation (') is used for complementary signals. In this example assume that the reference vector locates in Prism I Tetrahedron 1 and assume phase A carries the largest current. Fig. 7 also shows the voltage of phase A during the switching. Here V_{ap}, V_{as} and V_a are inverter output voltage, secondary voltage of transformer and filter output voltage, respectively. Similar sequence can be drawn for phases B and phase C.

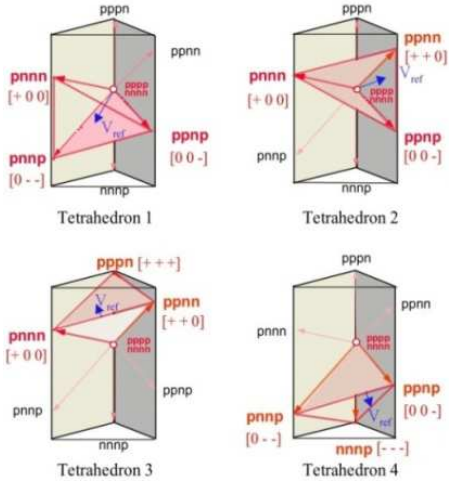


Fig.6. Presentation of the switching vector in the α-β-γ frame example for the reference vector located in prism1

TABLE III. Tetrahedron determination

Prism	Tetrahe-dron	ActiveVector			Reference vector component		
		V_1	V_2	V_3	V_{af}	V_{bf}	V_{cf}
P1	T1	ppnp	pnnp	pnnn	≥	<	<
	T2	pnnn	ppnn	ppnp	≥	≥	<
	T3	nnnp	pnnp	ppnp	≥	≥	≥
	T4	pppn	ppnn	pnnn	<	<	<
P2	T1	npnn	ppnn	ppnp	≥	≥	<
	T2	ppnp	npnp	npnn	<	≥	<
	T3	nnnp	npnp	ppnp	≥	≥	≥
	T4	pppn	ppnn	npnn	<	<	<
P3	T1	nppp	npnp	npnn	<	≥	<
	T2	npnn	nppn	nppp	<	≥	≥
	T3	pppn	nppn	npnn	≥	≥	≥
	T4	nnnp	npnp	nppp	<	<	<
P4	T1	nnpn	nppn	nppp	<	≥	≥
	T2	nppp	nnpp	nnpn	<	<	≥
	T3	pppn	nppn	nnpn	≥	≥	≥
	T4	nnnp	nnpp	nppp	<	<	<
P5	T1	pnpp	nnpp	nnpn	<	<	≥
	T2	nnpn	pnpn	pnpp	≥	<	≥
	T3	pppn	pnpn	nnpn	≥	≥	≥
	T4	nnnp	nnpp	pnpp	<	<	<
P6	T1	pnpp	pnnp	pnnn	≥	<	<
	T2	pnnn	pnpn	pnpp	≥	<	≥
	T3	pppn	pnpn	pnnn	≥	≥	≥
	T4	nnnp	pnnp	pnpp	<	<	<

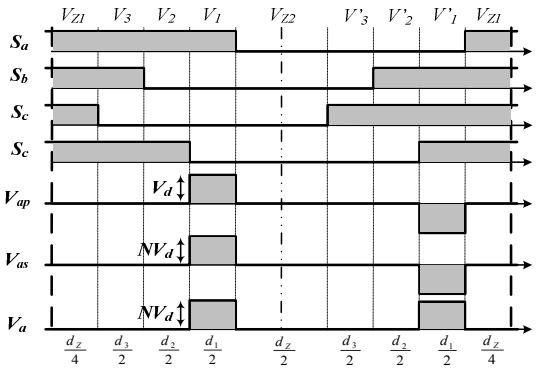


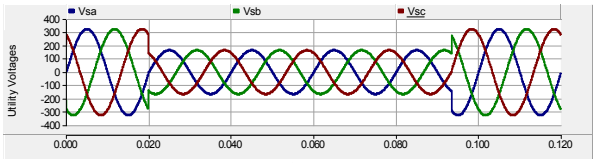
Fig. 7. The sequencing scheme of the proposed DVR

III. Simulation Results Conclusion

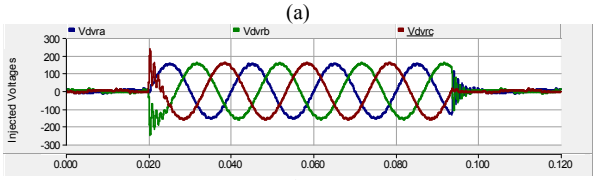
In this section, the proposed system in Fig.1 is simulated in PSCAD/EMTDC. System parameters are given Table IV. It should be noted that the series transformers are operating at switching frequency and in linear region. Fig. 8 shows the simulation results under balance voltage sag condition. In this case, 50% voltage sag has been considered for each phases. Utility voltage, injected voltage and load voltage are shown, respectively. It is clear that the load voltage is restored to the nominal condition (before sag occurrence) after a time lower than a half cycle. Fig. 9 shows the simulation results under unbalance voltage sag condition with the values of 60%, 50% and 40% on phases a, b, and c, respectively. As can be seen, under such conditions, this structure injects unbalance voltage in such a way that the load voltage remains balanced and sinusoidal and doesn't sense the voltage sag.

TABLE IV. System parameters

Parameters	*Value*
Line Frequency	50Hz
Switching frequency	10000Hz
Load voltage	230v rms
dc bus voltage	80v
Series transformer turns ratio	1:4
Filter inductance and capacitance	1mh & 25µf
Load a phase	45Ω, 40mh
Load b phase	60Ω, 30mh
Load c phase	90Ω, 70mh



(a)



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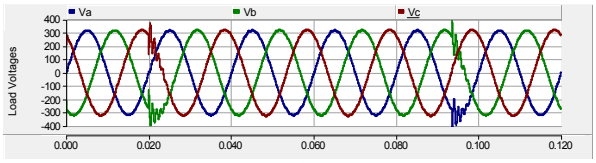
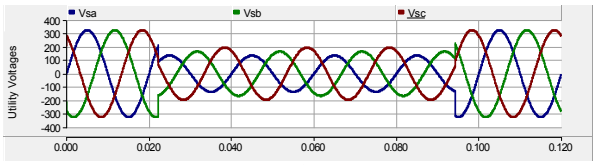
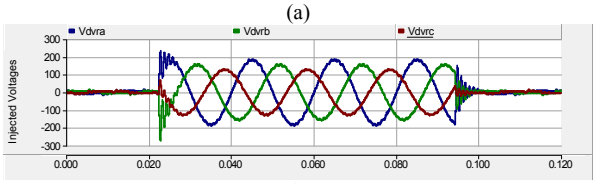


(c)

Fig.8. Simulation results under balanced sag (a) utility voltages (b) injected voltages (c) load voltages



(a)



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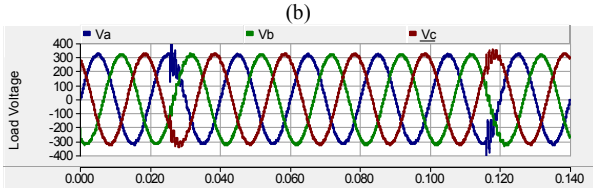
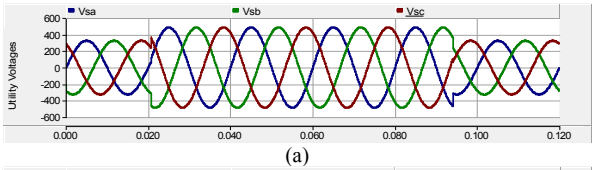


(c)

Fig.9. Simulation results under unbalanced voltage sag, (a) utility voltages (b) injected voltages (c) load voltages

In another case, the DVR performance is investigated under balanced and unbalanced voltage swell. Fig. 10 shows the performance of DVR under 50% balance voltage swell conditions. The results of unbalanced swell are shown in Fig. 11. In this case the three-phase terminal voltages with unbalanced swell of 60%, 50% and 40% on phase a, b, and c are considered, respectively. As can be seen, also under swell conditions, the load voltage is restored to its nominal value.



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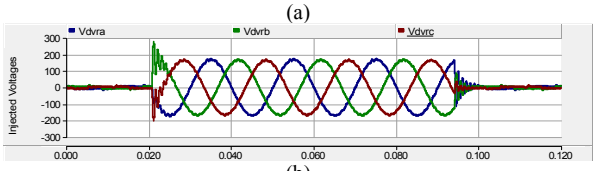

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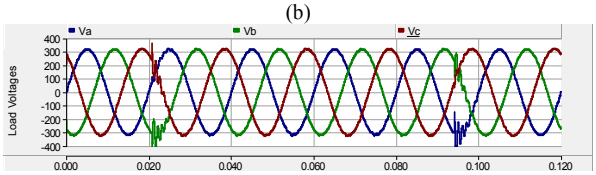

(c)

Fig.10. Simulation results under balance swell (a) utility voltages (b) injected voltages (c) load voltages

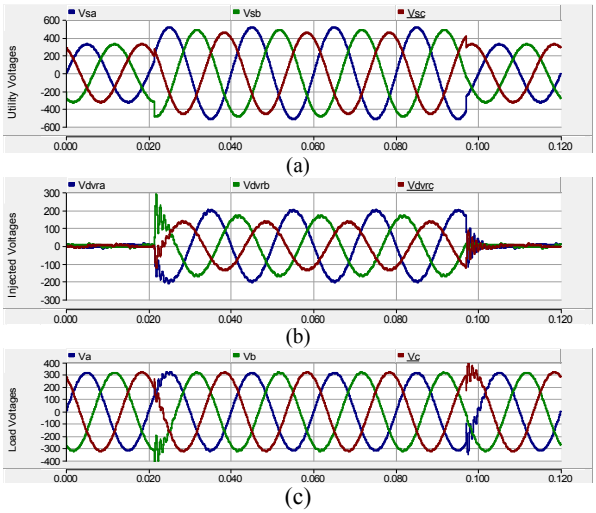

Fig.11. Simulation results under unbalanced swell (a) utility voltages (b) injected voltages (c) load voltages

Fig. 12 shows the simulation results of the proposed DVR under harmonic polluted utility voltage. It is clear that the load voltage remains balanced and sinusoidal even when such condition is occurred for utility voltage.

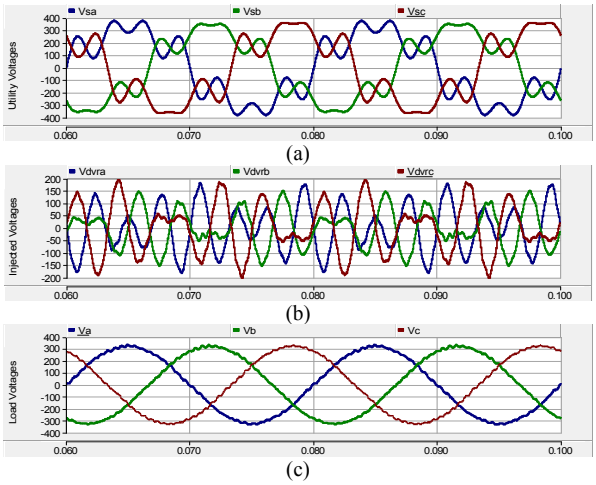

Fig.12. Simulation results under harmonic polluted utility voltage (a) utility voltages (b) injected voltages (c) load voltages

The THD values of utility voltages and load voltages compensated are given in TABLE V. The THD of the load voltage is less than 3% that lays in the criterion reported in IEEE standards 519-1992 [13].

TABLE V. THDs of utility and load voltages

	THD_a	THD_b	THD_c
Utility Voltage	%38.87	%32.02	%41.66
Load Voltage	%2.28	%1.91	%2.37

IV. Conclusion

In this paper, a three-phase four-wire PET based DVR was proposed for power quality improvement. From the structure point of view, the main advantage of the proposed DVR is low volume and weight due to use of PET. By applying the 3DSPVM control scheme, the proposed DVR was able to compensate voltage sag, voltage swell and also utility voltage harmonics for both balance and unbalance conditions. The proposed DVR performance was studied via simulation results in PSCAD/EMTDC software. The simulation results validated the satisfying operation of the proposed DVR.

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